Docket No.: P2000,0171

CERTIFICATION

I, the below named translator, hereby declare that: my name and post office address are as stated below; that I am knowledgeable in the English and German languages, and that I believe that the attached text is a true and complete translation of German Application No. 100 40 450.2, filed August 18, 2000.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Description

Memory cell arrangement

The present invention relates to a memory cell arrangement with read/write protection.

In the case of programmable integrated circuits, for example in the case of calibratable sensors, it may be desirable to protect the memory content of a nonvolatile memory after the one-time programming thereof in such a way that change or erasure is impossible.

The document US 6 041 007 A specifies an integrated circuit, preferably an electronic sensor, with a programmable memory cell designed as an EEPROM. In order to latch said memory cell, a latching memory cell is provided, which can be overwritten only when a signal that can be fed in externally is present. Reprogramming of the programmable memory cells is no longer possible after the conclusion of production.

One possibility for protecting the memory content consists in setting a write protection bit for latching the memory at the end of a one-time programming. This makes it possible to prevent further programming or activation of test routines and to latch a data input present at the integrated circuit. It is thus ensured that only one operating state, the so-called normal operating mode, can be implemented after the conclusion of programming and after the setting of the latching bit.

By way of example, by applying an overvoltage to voltage supply terminals of the integrated circuit, it is usually

possible to change from the normal operating mode to other modes, for example to a write mode, in which data are written to a nonvolatile memory. Furthermore, a test mode may be provided which enables a read-out of the nonvolatile memory, so that, by way of example, after each operation of writing a bit to the nonvolatile memory, it is possible to check whether this write operation has been effected in a manner free of errors.

In this case, however, the problem arises that if the latching bit is set in the nonvolatile memory, it is no longer possible to check that said write operation is free from errors, since only the normal operating mode can be implemented after the setting of the latching bit, said normal operating mode not permitting any test or read modes.

In particular, the problem can arise that when the latching bit is written in the nonvolatile memory, further memory cells of the nonvolatile memory are written to inadvertently. Such incorrect programming can remain undiscovered even in the event of extensive functional tests.

It is an object of the present invention to specify a memory cell arrangement in which latching of a nonvolatile memory is provided and in which the correct programming of a latched memory area can be checked.

The object is achieved by a memory cell arrangement, having
- a nonvolatile memory, which comprises a latching memory cell, which indicates a read and/or write protection of the nonvolatile memory, and
- a latching element, which is coupled to the nonvolatile memory, for preventing read and/or write operations on the nonvolatile memory, and

- an additional memory element, which, on the input side, is coupled to the latching memory cell and which, on the output side, is connected to the latching element in order to drive the latter.

In the case of the memory cell arrangement described, the latching of the nonvolatile memory is not effected directly by setting a bit thereof, rather the latching is effected by the additional memory element coupled to the latching element of the nonvolatile memory. The provision of such a latched copy of the latching memory cell of the nonvolatile memory, which copy can carry the latching bit (memory lock bit), enables, by way of example, a time-delayed activation of the additional memory element.

By way of example, depending on an operating mode of the memory cell arrangement, the memory content of the latching memory cell, which may be 1 bit, can be switched through to the output of the additional memory element and be continuously refreshed in a normal operating mode.

This makes it possible firstly to avoid inadvertent programming of the nonvolatile memory during operation due to latching thereof and also to check the freedom from errors in the programming operation with regard to the latching memory cell with a latching bit itself.

In an advantageous embodiment of the present invention, an activation element is provided, which effects a provision of information stored in the latching memory cell in the additional memory element in a manner dependent on an activation signal that can be fed to the activation element.

By way of example, a switch-on phase indicator signal may be able to be fed as activation signal to the activation element, said indicator signal being active during a switch-on phase of the memory cell arrangement or of an integrated circuit comprising the memory cell arrangement and thus indicating the switch-on phase.

By setting a latching bit in the latching memory cell, the nonvolatile memory in the memory cell arrangement is thus latched only when the memory cell arrangement is switched on a next time after a programming.

In a further advantageous embodiment of the present invention, an OR gate is provided, which, on the output side, is connected to an input of the activation element and to which, on the input side, a switch-on phase indicator signal and a normal operating mode indicator signal can be fed.

By feeding in a normal operating mode indicator signal in addition to a switch-on phase indicator signal, the nonvolatile memory can be latched as early as after the conclusion of the programming of the nonvolatile memory and the beginning of the normal operating mode of the memory cell arrangement. The possibility of checking the nonvolatile memory for error-free programming is preserved here.

In a further advantageous embodiment of the present invention, a decoding block is provided for the provision of the normal operating mode indicator signal, the output of which decoding block is connected to an input of the OR gate.

The decoding block can decode for example an increased operating voltage, which indicates a mode other than a normal operating mode and, in the case of a normal operating mode,

provide a normal operating mode indicator signal at its output.

In a further advantageous embodiment of the present invention, a D-type flip-flop is provided, which comprises the activation element and the additional memory element.

A D-type flip-flop enables a simple and reliable possibility for realizing the additional memory element and the activation thereof with an activation signal which can be fed to the clock input of the D-type flip-flop. In this case, the D input of the D-type flip-flop can be coupled to the latching memory cell.

In a further advantageous embodiment of the present invention, a volatile memory is provided, which has a data input and which, on the output side, is connected to the nonvolatile memory.

The data input of the volatile memory may be embodied as a serial data input. The data can be transferred in parallel from the volatile memory, which may be embodied as a register, to the nonvolatile memory. The latching element may be connected to the data input.

In a further advantageous embodiment of the present invention, the memory area of the volatile memory comprises a test register. The test register may be required in a test mode.

In a further advantageous embodiment of the present invention, the additional memory element is connected to a reset input of the test register on the output side. If a test register which can indicate an active test mode is provided, it is advantageous to reset the test register when the additional

memory element is activated. In this case, the data input of the volatile memory can be latched at the same time.

Further details of the present invention are specified in the subclaims.

The invention is explained in more detail below using an exemplary embodiment with reference to the drawing, in which:

The Fig. shows an exemplary embodiment of the memory cell arrangement using a block diagram.

The Fig. shows a volatile memory VM and a nonvolatile memory NM connected in parallel. The nonvolatile memory NM comprises a latching memory cell (memory lock) ML. The volatile memory VM, which serves for loading the nonvolatile memory NM, has a memory structure corresponding to that of the nonvolatile memory NM. In addition, however, the volatile memory VM has a test register TR. The volatile memory VM has a data input DI, which serves for the serial loading of said volatile memory. In this case, the latching bit for loading the latching memory cell ML is the last bit loaded into the volatile memory VM. Connected to the data input DI of the volatile memory VM is a latching element VE, which enables write operations, erase operations and read operations at the volatile memory VM and thus at the nonvolatile memory NM. The latching element VE is controlled by an additional memory element LH provided in a flip-flop FF. The flip-flop FF is designed as a D-type flip-flop to whose output the control input of the latching element VE is connected. The data input of the flip-flop FF is connected to the latching memory cell ML. The D-type flip-flop FF is embodied as a clock-state-controlled flip-flop FF which switches its input through to its output when a clock signal is present. For this purpose, the flip-flop FF has an

activation element AG connected to the output of an OR gate OR. A switch-on phase indicator signal PU and a normal operating mode indicator signal NO can be fed to said OR gate OR on the input side. For the provision of said normal operating mode indicator signal NO, a decoding block DB is connected to an input of the OR gate OR.

When data is fed in at the data input DI of the volatile memory VM when the memory cell arrangement is switched on for the first time, the latching bit in the latching memory cell ML is not yet set and, consequently, no latching of the data stream is active in the latching element VE. Accordingly, it is possible to carry out a read mode, for example, in which data are read from the data input DI into the volatile memory VM. Moreover, it is possible to execute a write mode, in which data are written from the volatile memory VM to the nonvolatile memory NM, and, finally, it is possible to execute a test mode, in which data are written from the data input DI to the test register TR. In these operating modes, a setting of the mem-lock bit in the latching memory cell ML does not have the effect that the latching element VE latches the data input DI of the volatile memory VM. This is because even if the mem-lock bit in the latching memory cell ML is set, it is not switched through to the output of the flip-flop since neither a switch-on phase indicator signal PU nor a normal operating mode indicator signal NO is present at the input of the activation element AG. Accordingly, the content of the nonvolatile memory NM can now be checked in a test mode, for example by readout via a current interface. Consequently, incorrect programmings of the nonvolatile memory NM can be precluded.

An activation of a normal operating mode causes a normal operating mode indicator signal NO to be available at the

output of the decoding block BD, which signal activates the flip-flop FF via the activation element AG in such a way that its input is switched through to its output and, consequently, a copy of the bit of the latching memory cell is available in the additional memory element LH, that is to say at the output of the flip-flop FF. This has the result that, with a set latching bit in the latching memory cell ML, firstly the latching element VE latches the data input DI and secondly the test TR is reset via the reset input RS. Consequently, the memory cell arrangement cannot subsequently be reprogrammed nor can the normal operating mode be interrupted. The feeding in of the switch-on phase indicator signal PU during a sufficiently long switch-on phase to the OR gate OR has the effect that the respective current memory content of the latching memory cell ML is taken over to the output of the flip-flop FF and thus into the additional memory element LH.

In order to leave a normal operating mode and activate a loading, test or write mode, an increased supply voltage can be applied to the memory cell arrangement. This overvoltage, which is desired for programming the memory cell arrangement, is undesirable, however, in a normal operating mode when interference signals activate the overvoltage mode. However, this does not jeopardize the operational reliability of the memory cell arrangement since, even if the normal operating mode indicator signal NO changes to the low state, the content of the additional memory element LH is frozen and the latching unit VE continues to latch the data input DI since the latching memory cell had already been programmed beforehand.

In an alternative embodiment, the OR gate OR could be omitted and the switch-on phase indicator signal PU could be feedable directly to the flip-flop FF. The decoding block DB and the OR gate OR can be omitted as a result of this, in which case

strong interference pulses of the supply voltage, during the operation of the memory cell arrangement, could lead to a cancellation of the latching in the latching element VE.

In order to increase the operational reliability with respect to overvoltage or undervoltage caused by interference pulses, the OR gate OR in accordance with the Fig. could be replaced by an OR gate with four inputs, to which the normal operating mode indicator signal NO can be fed at a first input, the switch-on phase indicator signal PU can be fed at a second input, an undervoltage indicator signal can be fed at a third input and, at a fourth input, the output of an AND gate can be fed in, to whose inputs firstly an overvoltage indicator signal and secondly the memory content of the additional memory element LH can be fed.

Instead of a memory map of the nonvolatile memory NM, the volatile memory VM may merely have an address which points to the nonvolatile memory or a further memory.

Instead of the D-type flip-flop FF, a positive edge triggered flip-flop, for example, could be used whose clock input could be driveable by a high-frequency clock signal only during the normal operating mode. Equally, the D-type flip-flop could be replaced by an RS flip-flop with corresponding additional gates.

Patent claims

1. A memory cell arrangement, having
- a nonvolatile memory (NM), which comprises a latching memory cell (ML), which indicates a read and/or write protection of the nonvolatile memory (NM),
- a latching element (VE), which is coupled to the nonvolatile memory (NM), for preventing read and/or write operations on the nonvolatile memory (NM), and
- an additional memory element (LH), which, on the input side, is coupled to the latching memory cell (ML) and which, on the output side, is connected to the latching element (VE) in order to drive the latter.

2. The memory cell arrangement as claimed in claim 1, characterized in that
an activation element (AG) is provided, which effects a provision of information stored in the latching memory cell (ML) in the additional memory element (LH) in a manner dependent on an activation signal that can be fed to the activation element (AG).

3. The memory cell arrangement as claimed in claim 2, characterized in that
an OR gate (OR) is provided, which, on the output side, is connected to an input of the activation element (AG) and to which, on the input side, a switch-on phase indicator signal (PU) and a normal operating mode indicator signal (NO) can be fed.

4. The memory cell arrangement as claimed in claim 3, characterized in that

a decoding block (DB) is provided for the provision of the normal operating mode indicator signal (NO), the output of which decoding block is connected to an input of the OR gate.

5. The memory cell arrangement as claimed in one of claims 2 to 4,
characterized in that
a D-type flip-flop (FF) is provided, which comprises the activation element (AG) and the additional memory element (LH).

6. The memory cell arrangement as claimed in one of claims 1 to 5,
characterized in that
a volatile memory (VM) is provided, which has a data input (DI) and which, on the output side, is connected to the nonvolatile memory (NM).

7. The memory cell arrangement as claimed in claim 6,
characterized in that
the volatile memory area (VM) comprises a test register (TR).

8. The memory cell arrangement as claimed in claim 7,
characterized in that
the additional memory element (LH) is connected to a reset input (RS) of the test register (TR) on the output side.

Abstract

Memory cell arrangement

A memory cell arrangement having a nonvolatile memory (NM), which can be latched by means of a latching element (VE), is specified. The nonvolatile memory (NM) is latched by activating a copy of the latching memory cell (LH), which is coupled to the latching memory cell (ML) and can be activated in a manner dependent on the operating state by means of an activation element (AG). This makes it possible to identify and avoid incorrect programmings, in particular in the case of calibratable sensors.

Figure